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Computer-Aided Large-Signal Measurement of IMPATT-Diode Electronic Admittance

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Abstract—**A technique for the measurement of the large-signal electronic admittance of IMPATT diodes as a function of frequency and RF voltage level using the network analyzer is described. The method de-embeds the admittance of the active region of the device from the mounting and measurement circuitry without physical disturbance of the diode. The small series resistance of the diode at breakdown is included in the embedding network together with the mount and diode package parameters. The determination of transformation networks between the measurement port and the active chip through a simple calibration procedure, a knowledge of the diode admittance below breakdown, and computer-aided optimization constitute the de-embedding procedure. Experimental electronic admittance curves are given for a low-power (100-mW) silicon IMPATT diode in the frequency range 5.7–6.5 GHz and with RF voltage levels applied across the active chip in the range 0–24 V, with an estimated error of less than 20 percent (typically 5 percent) in admittance values.**

I. Introduction

LARGE-SIGNAL characterization of an IMPATT diode *in situ* is essential to the investigation of nonlinear phenomena occurring in IMPATT-diode amplifiers. A fundamental problem in these measurements is deembedding the active-chip electronic admittance Y_e from the passive packaging and mounting network with its many parasitic reactances. This paper describes a rapid accurate technique for the measurement of large-signal IMPATT-diode electronic admittance as a function of RF voltage level and frequency. The method combines and refines the features of several published small-signal measurement procedures and extends them into the large-signal region, viz., 1) the use of a network analyzer for rapidity of measurement [1]–[3], [5], 2) direct transformation of electronic admittance to device terminal admittance [3]–[5], 3) determination of the transformation network without physical disturbance of the diode and circuit [3]–[6], 4) computer reduction of measured data [1]–[6], and 5) accuracy enhancement by the use of an optimization routine in the calibration and measurement process [3]–[5]. The present method is more accurate than the large-signal technique of Young and Stephenson [7] which does not incorporate features 2)–5).

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II. Experimental Setup

A schematic diagram of the admittance measurement setup is shown in Fig. 1. The measurement technique allows the diode under test to be operated in a microwave cavity under typical operating conditions while the measurements are carried out. For present purposes, the IMPATT diode is end-mounted in a precision 50-Ω coaxial cavity with movable slug tuning, although other configurations are also suitable. Constant bias current is applied

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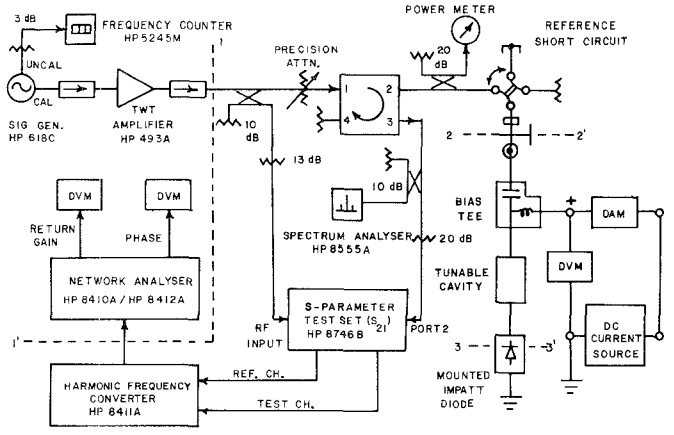

Fig. 1. Schematic diagram of the large-signal electronic admittance measurement setup.

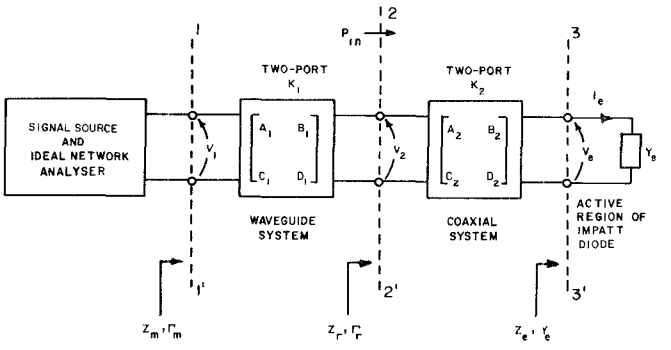

Fig. 2. Transformation of the IMPATT electronic admittance Y_e to the calibration reference plane 2–2′ and to the measurement reference plane 1–1′.

to the diode through a bias tee at the input of the coaxial cavity. The entire arrangement is connected via an adapter to a waveguide circulator and operated as a stable reflection amplifier. A waveguide switch is used to introduce a precision short circuit in order to monitor and adjust for drift in the measurement process. Directional couplers sample the input power P_{in} and the output power P_{out}. The spectrum analyzer is used to check that the output signal is spurious free. The input signal is generated by an isolated generator-TWT amplifier combination, producing a maximum 1-W signal which is adjusted by a precision attenuator. Prior to attenuation, the input signal is coupled to the RF input port of the S-parameter test set; the IMPATT amplifier output is fed to port 2 of the test set. Pads are used to keep the signal levels within operating range of the network analyzer. The network analyzer compares these two signals and displays the measured return gain and phase, from which the measured complex reflection coefficient Γ_m and impedance Z_m can be calculated. With this setup the network analyzer's normal range of operation, in the small-signal region, is extended to the large-signal region.

Three reference planes are delineated in Fig. 1.

1) Plane 1–1′, the reference plane for measurement of Γ_m or Z_m without calibration, is situated inside the network analyzer.

2) Plane 2–2′, the reference plane for impedance measurements Γ_r or Z_r, is at the same plane as the reference short circuit.

3) Plane 3–3′, the terminal plane for the electronic admittance Y_e, is inside the diode package.

The reference plane 2–2′ is required so that the input and output powers measured there can be related to the RF voltage across the active diode chip. Planes 2–2′ and 3–3′ must be established by suitable calibration procedures.

III. Theory for the Deembedding Procedure

An equivalent circuit for the measurement setup is shown in Fig. 2. The planes 1–1′, 2–2′, and 3–3′ demarcate the components for RF-signal generation and analysis (assumed ideal), the waveguide measurement system, the coaxial system, and the active region of the IMPATT diode, respectively, corresponding to their locations in Fig. 1. The analysis of the equivalent circuit is based on the use of $ABCD$ transmission parameters representing the two-port networks K_1 and K_2.

The determination of matrix K_1 is a calibration process utilizing a waveguide precision movable short circuit having a reflection coefficient given by

$$\Gamma_{s_i} = -1\exp(-j2\beta l_i), \qquad i=1,2,\cdots,N, \quad N\geqslant 3 \tag{1}$$

for N offsets $l_1, l_2, \cdots, l_N$ of the movable short from plane 2–2′, where $\beta = 2\pi/\lambda_g$ is the phase constant for the waveguide, $\lambda_g = \lambda_0/(1-(\lambda_0/\lambda_c)^2)^{1/2}$ is the guide wavelength, $\lambda_0 = c/f$ is the free-space wavelength, λ_c is the cutoff wavelength, $c = 2.998\times 10^{10}$ cm/s, and f is the frequency of measurement. With the short circuit connected at plane 2–2′, the measured reflection coefficient is given by the bilinear transformation:

$$\Gamma_{m_i} = \frac{a_1'\Gamma_{s_i} + b_1'}{c_1'\Gamma_{s_i} + 1}, \qquad i=1,2,\cdots,N, \qquad N\geqslant 3 \tag{2}$$

where the $[a_1'b_1'c_1']$ are normalized algebraic functions of the conventional $[A_1B_1C_1D_1]$ parameters for network K_1. The "best" values for a_1', b_1', and c_1' are determined by using a Fletcher–Powell optimization routine together with the mean-squared error objective function given by

$$U[K_1] = \min\left\{\frac{1}{N}\sum_{i=1}^{N}\left|\Gamma_{m_i} - \left(\frac{a_1'\Gamma_{s_i} + b_1'}{c_1'\Gamma_{s_i}+1}\right)\right|^2\right\}. \tag{3}$$

Knowledge of $K_1[a_1'b_1'c_1']$ at each frequency permits all subsequent measurements on unknown impedances to be referenced to plane 2–2′ by the inverse bilinear transformation:

$$\Gamma_r = \frac{b_1' - \Gamma_m}{c_1'\Gamma_m - a_1'} \tag{4}$$

where Γ_r is the actual reflection coefficient and Γ_m is measured. Then

$$\tilde{Z}_r = \frac{Z_r}{Z_0} = \frac{1+\Gamma_r}{1-\Gamma_r} = \frac{1}{\tilde{Y}_r} \tag{5}$$

is the normalized impedance, referred to plane 2–2′. If plane 2–2′ is in a coaxial medium then the characteristic impedance Z_0 is known; Z_0 is not known in waveguide, but it is not required since normalized waveguide impedances are used throughout the rest of the deembedding procedure.

Terminals 3–3′ are not accessible for the substitution of usual calibration standards if the IMPATT diode is to be measured *in situ*. However, the electronic impedance Z_e of the diode below breakdown can be used to determine the network $K_2[A_2B_2C_2D_2]$. In reverse bias, below breakdown voltage V_B, the electronic impedance is

$$Z_e(V_i)=R_s(V_i)-jX_d(V_i), \qquad i=1,2,\cdots,M, \qquad M\geqslant 3 \tag{6}$$

where V_i is the reverse bias voltage ($V_i<V_B$), $R_s(V_i)$ is the series resistance of the unswept region, $X_d=1/\omega C_d$ is the reactance of the depletion layer, and $C_d(V_i)$ is the capacitance of the depletion layer measured as a function of voltage on a 1-MHz capacitance bridge. The series resistance $R_s(V_i)$ is calculated from the low-frequency C_d-V data [6], assuming $R_s(V_B)$ to be zero; i.e., above breakdown all inactive regions of the IMPATT diode are lumped into the network K_2. Since the active region width (typically 10 μm) is very small compared to wavelength at RF frequencies, R_s and C_d are assumed to be independent of frequency well into the microwave region.

Microwave impedance measurements on the IMPATT amplifier in Fig. 1, at the same reverse bias voltages below breakdown at which $Z_e(V)$ was measured, are used to determine $K_2[A_2B_2C_2D_2]$. For the load $Z_e(V_i)$, the bilinear transformation

$$\tilde{Z}_r(V_i)=\frac{a_2Z_e(V_i)+b_2}{c_2Z_e(V_i)+1}, \qquad i=1,2,\cdots,M \tag{7}$$

can be used where $\tilde{Z}_r(V_i)$ is determined from (5) and $a_2=A_2/Z_0D_2$, $b_2=B_2/Z_0D_2$, and $c_2=C_2D_2$ are normalized transmission parameters for network K_2. Since network K_2 is reciprocal, we can write

$$A_2D_2-B_2C_2=1=Z_0D_2^2(a_2-b_2c_2). \tag{8}$$

As before, the "best" values for a_2, b_2, and c_2 are found by minimizing the objective function

$$U[K_2]=\min\left\{\frac{1}{M}\sum_{i=1}^{M}\left|\tilde{Z}_r(V_i)-\left(\frac{a_2Z_e(V_i)+b_2}{c_2Z_e(V_i)+1}\right)\right|^2\right\}. \tag{9}$$

The determination of $K_1[a_1'b_1'c_1']$ and $K_2[a_2b_2c_2]$ at each frequency completes the deembedding procedure.

Above the breakdown voltage the diode breaks into avalanche and operates in the normal IMPATT mode. The impedance $\tilde{Z}_r(V_{RF})$ is calculated from complex reflex coefficient measurements Γ_m measured at plane 1–1′ and transformed to plane 2–2′ via $K_1[a_1'b_1'c_1']$ using (4) and (5). Here V_{RF} is the RF voltage across the active region of the IMPATT diode. The electronic admittance $Y_e(V_{RF})$ at constant dc current and RF frequency is then given by the inverse mapping of (7), that is

$$Y_e(V_{RF})=\frac{c_2\tilde{Z}_r(V_{RF})-a_2}{b_2-\tilde{Z}_r(V_{RF})}=G_e(V_{RF})+jB_e(V_{RF}) \tag{10}$$

where $G_e(V_{RF})$ and $B_e(V_{RF})$ are the conductance and susceptance, respectively, of the diode's active region at an RF voltage level V_{RF}. The RF voltage is calculated from [4]

$$V_{RF}=\frac{(8P_{in}|a_2-b_2c_2|)^{1/2}}{|(b_2+1)Y_e(V_{RF})+a_2+c_2|}. \tag{11}$$

IV. Experimental Results

The measurement of total diode capacitance at 1 MHz includes the effects of parasitics in the diode package. An equivalent circuit for the diode package is a π network consisting of a shunt package capacitance C_p, series mesh and post inductance L_p, and shunt fringing capacitance C_f associated with the bonding wires near the diode chip [6], [8], [9]. At 1 MHz the reactance of L_p is negligible and $X_d\gg R_s$, so that the measured capacitance $C_m(V)$ at an applied reverse bias voltage V below breakdown is [5], [8]

$$C_m(V)=C_p+C_f+C_d(V). \tag{12}$$

For a one-sided abrupt junction device, the depletion-layer capacitance is given by [8]

$$C_d(V)=C_d(0)(1+V/\phi)^{-1/2} \tag{13}$$

where $C_d(0)$ is the capacitance at zero bias and ϕ is the built-in junction potential. Equations (12) and (13) yield

$$C_d^{-2}(V)=\left[C_m(V)-(C_p+C_f)\right]^{-2}=C_d^{-2}(0)(1+V/\phi). \tag{14}$$

Thus to a good approximation, the parasitic capacitance C_p+C_f is that value which when subtracted from measured capacitance results in $C_d^{-2}(V)$ which is a linear function of reverse bias voltage V. The approximate value for C_p+C_f obtained in this manner can be compared with independent measurements of C_p and C_f to assess the suitability of the assumed package π model. The package capacitance C_p can be measured for an empty diode package. The fringing capacitance C_f can be obtained by subtracting C_p from the capacitance of a diode package with the semiconductor chip removed and with the bonding wires in place at the normal height of the chip.

The experimental IMPATT diode was a 100-mW silicon p^+-n-n^+ device, Hewlett-Packard type HP-5082-0431 in package style 41. The breakdown voltage of the experimental diode was near 101 V dc. Therefore, 13 capacitance measurements ($M=13$) were made on a 1-MHz capacitance bridge (Boonton model 71A) at reverse bias voltages in the range 0–100 V dc. The bridge was initially nulled with the jig which supports the diode to account for stray capacitance in the jig. From the measured diode capacitance the approximate parasitic capacitance C_p+C_f was found to be 0.26 pF. A package capacitance C_p of 0.28 pF was measured by connecting an empty diode package in the supporting jig in place of the packaged

diode. Comparison of these results suggests that the fringing capacitance is only a very small fraction of the package capacitance and that C_f can be considered, for convenience, part of the diode impedance. Thus the equivalent circuit for the package can be simplified to an LC network consisting of shunt package capacitance C_p together with series lead inductance L_p. Since the package used is a low-pedestal type (in which the pedestal extends only one-third the height of the ceramic cylindrical envelope) the assumption of a simple LC package coupling circuit agrees with published work on a low-pedestal S-4 type package [9]. The package capacitance was then subtracted from the measured capacitance values to obtain values of junction capacitance. Fig. 3 shows the measured depletion-layer capacitance and calculated series resistance of the unswept region as a function of reverse bias.

Due to the need for high sensitivity in return gain and phase, excessive drift of the network analyzer posed a difficult problem for sufficient precision to be attained. Also, Γ_m was found to vary greatly with the signal power incident on a constant test load. Adding the waveguide switch in Fig. 1 solved these problems. One path in Fig. 1 is the normal path for diode measurements; the alternate path is terminated by a precision short circuit. This short circuit served as a calibration reference for every measurement Γ_m, i.e., all measurements were referred to the same impedance and could be compared absolutely regardless of the drift of the network analyzer or of any other slow changes in the complete setup. Mechanical switching between the two paths was found to be very reproducible.

To extract matrix K_1 at each frequency, 10 reflection measurements ($N = 10$) were performed with offsets of the short circuit connected at plane 2–2′ in the range 0–0.50 in.

After the diode was mounted in the cavity, 25 mA dc bias current was applied, and the IMPATT amplifier was tuned for 10-dB small-signal gain at the desired measurement frequency over a 1-dB bandwidth of about 50 MHz. Reflection coefficient measurements were then made on the amplifier assembly with the diode biased below breakdown at the same 13 voltages as for the 1-MHz capacitance measurements. Using the data in Fig. 3, computer reduction of the measured data yielded the matrix K_2 at each frequency.

With the diode biased above breakdown, at constant 25-mA bias current, reflection coefficient measurements at varying incident RF power (-20 to $+23$ dBm) yielded the large-signal electronic admittance Y_e. The measured dependence of the large-signal electronic admittance on frequency and on drive signal is illustrated in Fig. 4. It can be seen that $|G_e|$ decreases with increasing signal level, resulting in a decrease in amplifier gain, but is relatively independent of frequency. Also, $|B_e|$ increases with increasing signal level and also with increasing frequency, tending to shift the amplifier center frequency downwards. A conservative error analysis yields an error estimate of about 20 percent for the large-signal electronic

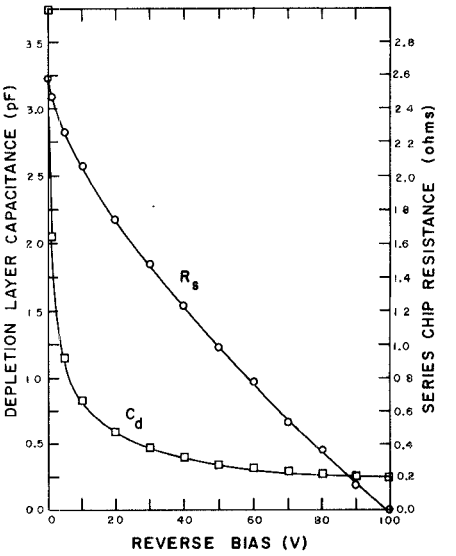

Fig. 3. Series resistance and depletion-layer capacitance of the active region of the experimental IMPATT diode below breakdown voltage.

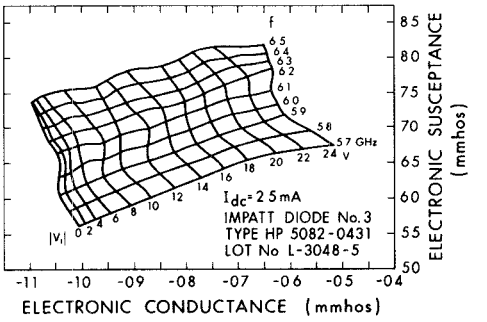

Fig. 4. Frequency and RF voltage behavior of the large-signal electronic admittance of the experimental IMPATT diode.

admittance [10]. However, through the use of redundant data and least squares optimization, the measurement error in practice is much less than this estimate, and is typically in the order of 5 percent, as obtained from examination of the fine admittance grid spacing achieved in Fig. 4. Indeed, theoretical intermodulation distortion studies [11] using the measured electronic admittance agree within 5 percent with measured intermodulation results.

If the total diode impedance of both active and passive regions is required, the series resistance of the diode at breakdown (which includes spreading resistance, contact resistance, and the resistance of unswept regions) must be added to the electronic impedance. This series resistance is not determined using the present method, but is in the order of 1 Ω or less than 5 percent of the electronic resistance.

V. Conclusions

A method is developed here for the accurate measurement of IMPATT-diode large-signal electronic admittance, using a network analyzer and computer-aided data reduction techniques. The method allows measurement of the admittance with the IMPATT diode *in situ*, thereby includ-

ing and accounting for the effects of external circuitry and package parasitic elements without the substitution of dummy diode calibration standards. This extraction of the electronic admittance isolates the diode nonlinearities and simplifies further studies on the effects of such nonlinearities on IMPATT-amplifier behavior. Other advantages of the method are speed and ease of changing measurement frequency. The large-signal admittance measurement setup described is suitable as long as harmonic voltages across the diode are negligibly small compared with the fundamental. This condition ensures that amplitude and phase measurements at the fundamental frequency are not distorted. The present setup can be modified for general large-signal operations by adding low-pass filters at the fundamental so that any harmonic frequencies present are attenuated before reaching the network analyzer. The estimated error in the measurement of electronic admittance is less than 20 percent, and is thought typically to be about 5 percent. The method is not as accurate as the time-consuming single-frequency method of van Iperen and Tjassens [9], but is considered to be more accurate than other published multifrequency methods.

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Simulation of Nonlinear Microwave FET Performance Using a Quasi-Static Model

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***Abstract*—A technique is described for accurately predicting nonlinear performance of microwave GaAs field-effect transistors in arbitrary circuit embedding. The approach is based on a quasi-static device model which is derived from measured bias and frequency dependence of the small-signal device *S* parameters. Excellent agreement is demonstrated between experimental and predicted "load-pull" characteristics at *X* band.**

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I. INTRODUCTION

THE achievements in device fabrication over the past years have made the GaAs FET attractive for a wide variety of microwave applications. Emphasis has been on wide-band amplifiers, both for large-signal as well as for highly linear small-signal low-noise operation. Increasing interest has also been devoted to employing GaAs FET's in voltage-tuned oscillators, frequency multipliers, and mixers. The nonlinear behavior of a device in a particular application is determined to a large extent by